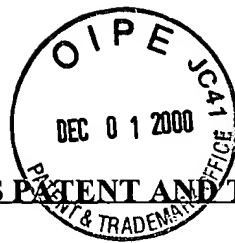


S/N 09/691,004



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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Unknown

Serial No.: 09/691,004

Group Art Unit: Unknown

Filed: October 18, 2000

Docket: 303.324US4

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND
METHODS OF FABRICATION AND USE

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Please charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date

27 November 2000

By

Robert E. Mates
Reg. No. 35,271

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 28 day of November, 2000.

Gina M. Uphus

Name

Signature

Gina Uphus